Parent Cls 22-30 & 38

MARKED UP CLAIMS ARE AS FOLLOWS

1-21. (Cancelled)

22. (Currently Amended) An instruction set architecture to convert voice and data samples into packets for transmission over a network and to convert packets received from the network into voice and data samples, the instruction set architecture comprising:

a plurality of digital signal processing (DSP) instructions for performing DSP operations within a processor, the plurality of DSP instructions accessing at least a first operand and a second operand to perform the instruction and writing a result upon completion, the plurality of DSP instructions including,

a 20-bit DSP instruction, and

a 40-bit DSP instruction;

and

a plurality of control instructions for controlling the execution of the plurality of DSP instructions, the plurality of control instructions including,

a 20-bit control instruction, and

a 40-bit control instruction.

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23. (Previously Added) The instruction set architecture of claim 22, wherein,

the plurality of DSP instructions to perform DSP operations within a plurality of core digital signal processors, and

the plurality of control instructions executed by a RISC processor to control the DSP operations within the plurality of core digital signal processors.

24. (Previously Added) The instruction set architecture of claim 22, wherein,

the 40-bit DSP instruction and the 20-bit control instruction include bits to perform execution prediction.

25. (Previously Added) The instruction set architecture of claim 24, wherein,

execution prediction depends upon a condition to change instruction execution.

26. (Previously Added) The instruction set architecture of

claim 22, wherein,

the 40-bit DSP instruction include bits to access operands in memory and registers.

27. (Currently Amended) An ~~The~~ instruction set architecture to convert voice and data samples into packets for transmission over a network and to convert packets received from the network into voice and data samples, the instruction set architecture comprising: ~~of claim 22, wherein,~~

a plurality of digital signal processing (DSP) instructions for performing DSP operations within a processor, the plurality of DSP instructions accessing at least a first operand and a second operand to perform the instruction and writing a result upon completion, the plurality of DSP instructions including,

a 20-bit DSP instruction, wherein at least one of the 20-bit DSP instructions is a dyadic DSP instruction including a main digital signal processing operation and a sub digital signal processing operation;

and

a 40-bit DSP instruction;

and

a plurality of control instructions for controlling the execution of the plurality of DSP instructions, the plurality of control instructions including,

a 20-bit control instruction, and

a 40-bit control instruction.

28. (Previously Added) The instruction set architecture of claim 27, wherein

the digital signal processing operations are of the set of operations of multiplication, addition, extremum, and no operation.

29. (Currently Amended) An ~~The~~ instruction set architecture to convert voice and data samples into packets for transmission over a network and to convert packets received from the network into voice and data samples, the instruction set architecture comprising: ~~of claim 22, wherein,~~

a plurality of digital signal processing (DSP) instructions for performing DSP operations within a processor, the plurality of DSP instructions accessing at least a first operand and a second operand to perform the instruction and writing a result upon completion, the

plurality of DSP instructions including,

a 20-bit DSP instruction, and

a 40-bit DSP instruction, wherein at least one of the 40-bit DSP instructions is a dyadic DSP instruction including a main digital signal processing operation and a sub digital signal processing operation;

and

a plurality of control instructions for controlling the execution of the plurality of DSP instructions, the plurality of control instructions including,

a 20-bit control instruction, and

a 40-bit control instruction.

30. (Previously Added) The instruction set architecture of claim 29, wherein

the digital signal processing operations are of the set of operations of multiplication, addition, extremum, and no operation.

31. (Currently Amended) An instruction set architecture of an application specific signal processor to convert voice and data samples into packets for transmission over a network and to

a 20-bit dyadic DSP instruction,

a 40-bit dyadic DSP instruction, and

wherein the 20-bit dyadic DSP instruction and the 40-bit dyadic DSP instruction include a main digital signal processing operation and a sub digital signal processing operation;

and

a control instruction set architecture for a RISC control unit to control the execution of DSP instructions by the plurality of signal processing units.

37. (Previously Added) The instruction set architecture of claim 36, wherein

the digital signal processing operations are of the set of operations of multiplication, addition, extremum, and no operation.

38. (Currently Amended) An instruction set architecture (ISA) for execution of operations within a digital signal processor to convert voice and data samples into packets for transmission over a network and to convert packets received from

the network into voice and data samples, the instruction set architecture comprising:

a set of digital signal processing (DSP) instructions for operation within a digital signal processor wherein each DSP instruction includes a first operand accessed directly from memory, a second operand accessed directly from memory of a local register, and a destination register to store results, the set of DSP instructions including,

a twenty bit DSP instruction, and

a forty bit DSP instruction,

the set of DSP instructions to accelerate calculations within the digital signal processor of the type where D = [(A operation one B) operation two C] where operation one and operation two are separate signal processing operations

and

a set of control instructions for controlling the execution of the set of DSP instructions, the set of control instructions including,

a twenty bit control instruction, and

a forty bit control instruction.

39. (Previously Added) The instruction set architecture (ISA) of claim 38 for execution of operations within a digital signal processor, wherein,

the twenty bit DSP instruction uses mode bits in control registers and

the forty bit DSP instruction has a control extension to override the mode bits.

40. (Previously Added) The instruction set architecture (ISA) of claim 38 for execution of operations within a digital signal processor, wherein,

the set of instructions further includes a dyadic instruction to execute two operations in one instruction.

41. (Previously Added) The instruction set architecture (ISA) of claim 40 for execution of operations within a digital signal processor, wherein

the two operations of the dyadic instruction for execution in one instruction are DSP operations.

42. (Previously Added) The instruction set architecture

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-8, drawn to a processor with a set of multiplier and adder for processing main operation of a dyadic instruction and anothher set for processing sub-operation, classified in class 708, subclass 501.

II. Claims 9-13, drawn to a method of processing dyadic instructions by decoding to generate signals to select inputs of multiplexers of functional blocks, classified in class 712, subclass 208

III. Claims 14-19, drawn to an instruction set architecture for executing dyadic instruction for calculating the specific type of D=(A op1 B) op2 C, classified in class 712, subclass 221.

IV. Claims 19 and 20, drawn to a dyadic instruction with a field indicating sequential or parallel execution of main and sub operations, classified in class 712, subclass 200.

2. The inventions are distinct, each from the other because of the following reasons:

Inventions of group I and groups II, II, and IV are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the invention of group I can be used in a system without the functional block multiplexer input

1. Claims 14-18 and 21-37 are presented for examination.

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 14-18 and 21, drawn to an instruction set architecture including instructions to perform (A op1 B) op2 C function, classified in class 712, subclass 200.

   II. Claims 22-37, drawn to an instruction set architecture including control instructions, classified in class 712, subclass 200.

3. The inventions are distinct, each from the other because of the following reasons:

Inventions of Group i and Group II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the invention of Group I can be used in a system without the control instructions. The subcombination has separate utility such as use in a system without the (A op1 B) op2 C processing instruction.

4. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

1. Claims 22-44 remain for examination

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 22-30 and 38-43, drawn to an Instruction Set Architecture with 20 and 40 bit control instructions for controlling execution of DSP instructions, classified in class 712, subclass 200.

   II. Claims 31-37 and 44, drawn to an Instruction Set Architecture with control instructions for RISC control unit to control execution of DSP instructions in a plurality of DSP units, classified in class 712, subclass 200.

3. The inventions are distinct, each from the other because of the following reasons:

Inventions of group I and group II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the invention of group I can be used in a system without the RISC control unit. The subcombination has separate utility such as use in a system without the 20 and 40 bit control instructions.

4. Because these inventions are distinct for the reasons given above and the search required for one group is not required for the other group, restriction for examination purposes as indicated is proper.

1. Claims 22-30, 38-43, and 45-49 remain for examination.

2. Applicant is reminded that the new claims 44-48 have been renumbered to claims 45-49.

3. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 22-26 and 45-49, drawn to an instruction set architecture for executing instructions in RISC processor to control DSP instruction execution in DSP processor cores, classified in class 700, subclass 3.

II. Claims 27-30 and 38-43, drawn to an instruction set architecture for executing control instructions to control execution of dyadic DSP instructions, classified in class 712, subclass 221.

4. The inventions are distinct, each from the other because of the following reasons: Inventions *of Group I* and *Group II* are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because *the invention of group I can be used in a system without the dyadic DSP instruction processing*. The subcombination has separate utility such as *use in a system without the control instruction executed in a RISC processor.*

5. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification and the search required for one group is not required for the other group, restriction for examination purposes as indicated is proper.

6. Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

7. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one

1. Claims 14-18 and 21-29 are presented for examination.

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 14-18 and 21, drawn to a DSP instruction set architecture of type D={[A Op1 B] Op2 C} in 20 bit and 40 bit format, classified in class 712, subclass 223.

   II. Claims 23-29, drawn to a DSP instruction set architecture with RISC unit control instructions to control execution of DSP instructions, classified in class 712, subclass 35.

3. The inventions are distinct, each from the other because of the following reasons: Inventions *Group I* and *Group II* are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because *the invention of group I can be used in a system without the RISC unit control instructions to control DSP operations.* The subcombination has separate utility such as *use in a system without instruction type of D={[A Op1 B] Op2 C}.*

4. Because these inventions are distinct for the reasons given above and the search required for *one group* is not required for *the other group,* restriction for examination purposes as indicated is proper.

5. Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

6. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).